What is claimed is:

[Claim 1] 1. A method of IP characterization, comprising:

providing an IP component;

automatically generating a plurality of test patterns for all paths in the IP component;

sequentially inputting the test patterns into the IP component for simulation, and outputting a plurality of corresponding simulation results; and

generating an IP characteristic library based on the simulation results.

[Claim 2] 2. The method of IP characterization of claim 1, wherein the step of automatically generating the plurality of test patterns for all paths in the IP component comprises:

automatically searching all of the paths in the IP component; and

generating the corresponding test patterns for each of the paths.

[Claim 3] 3. The method of IP characterization of claim 2, wherein the step of automatically searching all of the paths in the IP component comprises:

identifying and excluding an ESD path;

wherein if there is at least a path point which has not been completely searched, the path point is selected;

determining whether one of the paths of the selected path point reaches an end point of the path or not;

searching a next path point connected by one of the paths of the selected path point by selecting a connection terminal of a transistor based on a transistor rule; and

searching a next path point connected by one of the paths of the selected path point by selecting a connection terminal of a resistor based on a resistor rule.

[Claim 4] 4. The method of IP characterization of claim 3, wherein the step of automatically searching all of the paths in the IP component further comprises:

analyzing a type of all of the I/O ports in the IP component; and

comparing the I/O ports of the IP component with an I/O port information stored in a database.

[Claim 5] 5. The method of IP characterization of claim 4, wherein the type of the I/O ports comprises an input port, an output port and a bi-directional port.

[Claim 6] 6. The method for IP characterization of claim 3, wherein the step of automatically searching all of the paths in the IP component further comprises excluding any path which is input/output from any of the I/O ports in the IP component not passing through any circuitry in the IP component.

[Claim 7] 7. The method of IP characterization of claim 1, wherein the step of generating the IP characteristic library based on the simulation results comprises:

extracting at least one key data from each of the simulation results, respectively; and

integrating the key data of each of the simulation results to generate the IP characteristic library.

[Claim 8] 8. The method of IP characterization of claim 1, wherein the IP characteristic library comprises a plurality of timing information and a plurality of power information corresponding to the test patterns.

[Claim 9] 9. The method for IP characterization of claim 1, wherein the IP component is configured by a Hardware Description Language (HDL).

[Claim 10] 10. A method of finding paths in IP component, comprising:

providing an IP component;

identifying and excluding an ESD path;

wherein if there is at least a path point which has not been completely searched yet, the path point is selected;

determining whether or not one of the paths of the selected path point reaches an end point of the path;

searching a next path point connected by one of the paths of the selected path point by selecting a connection terminal of a transistor based on a transistor rule; and

searching a next path point connected by one of the paths of the selected path point by selecting a connection terminal of a resistor based on a resistor rule.

[Claim 11] 11. The method of finding paths in IP component of claim 10, further comprising:

analyzing a type of all of the I/O ports in the IP component; and

comparing the I/O ports of the IP component with an I/O port information stored in a database.

[Claim 12] 12. The method of finding paths in IP component of claim 11, wherein a type of the I/O ports comprises an input port, an output port and a bi-directional port.

[Claim 13] 13. The method of finding paths in IP component of claim 10, further comprising excluding any path which is input/output from any of the I/O ports in the IP component not passing through any circuitry in the IP component.

[Claim 14] 14. The method of finding paths in IP component of claim 10, wherein the IP component is configured by a Hardware Description Language (HDL).

[Claim 15] 15. A computer readable recording media for storing a program implemented by a computer system, the program comprising a plurality of following instructions:

reading an IP component;

automatically generating a plurality of test patterns for all paths in the IP component;

sequentially reading each of the test patterns for performing simulation on the IP component and generating a plurality of corresponding simulation results; and

generating an IP characteristic library based on the simulation results.

[Claim 16] 16. The computer readable recording media of claim 15, wherein the instruction of automatically generating the plurality of test

patterns for all paths in the IP component comprises a plurality of following instructions:

automatically searching all of the paths in the IP component; and

generating the corresponding test patterns for each of the paths.

[Claim 17] 17. The computer readable recording media of claim 16, wherein the instruction of automatically searching all of the paths in the IP component comprises:

identifying and excluding an ESD path;

wherein if there is at least a path point which has not been completely searched, the path point is selected;

determining whether or not one of the paths of the selected path point reaches an end point of the path;

searching a next path point connected by one of the paths of the selected path point by selecting a connection terminal of a transistor based on a transistor rule; and

searching a next path point connected by one of the paths of the selected path point by selecting a connection terminal of a resistor based on a resistor rule.

[Claim 18] 18. The computer readable recording media of claim 17, wherein the instruction of automatically searching all of the paths in the IP component further comprises:

analyzing a type of all of the I/O ports in the IP component; and

comparing the I/O ports of the IP component with an I/O port information stored in a database.

[Claim 19] 19. The computer readable recording media of claim 18, wherein a type of the I/O ports comprises an input port, an output port and a bi-directional port.

[Claim 20] 20. The computer readable recording media of claim 17, wherein the instruction of automatically searching all of the paths in the IP component further comprises excluding any path which is input/output from

any of the I/O ports in the IP component and not passed through any circuitry in the IP component.

[Claim 21] 21. The computer readable recording media of claim 15, wherein the instruction of generating the IP characteristic library based on the simulation results comprises:

extracting at least one key data from each of the simulation results, respectively; and

integrating the key data of each of the simulation results to generate the IP characteristic library.

[Claim 22] 22. The computer readable recording media of claim 15, wherein the IP characteristic library comprises a plurality of timing information and a plurality of power information corresponding to the test patterns.

[Claim 23] 23. The computer readable recording media of claim 15, wherein the IP component is configured by a Hardware Description Language (HDL).